REMARKS

Claims 1-12, 21-24 and 28-38 are all of the claims presently pending in the application. The claims have not been amended by the present response. Claims 36-38 have been added to provide more varied protection for the claimed invention and to claim additional features of the invention.

Claims 1-12, 21-24 and 28-35 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Joshi et al. (U.S. Patent No. 6,921,982; hereinafter "Joshi").

This rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention of exemplary claim 1 is directed to a double-gate field effect transistor.

The transistor includes a strained-silicon channel formed adjacent a source and a drain, a first gate formed over a first side of the channel, a second gate formed over a second side of the channel, a first gate dielectric formed between the first gate and the strained-silicon channel and a second gate dielectric formed between the second gate and the strained-silicon channel (e.g., see Application at page 3, lines 8-14).

II. THE PRIOR ART REFERENCE

The Examiner alleges that Joshi teaches the claimed invention of claims 1-12, 21-24 and 28-33. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Joshi.

That is, Joshi does not teach or suggest "*a double-gate field effect transistor*", as recited in claim 1, and similarly recited in claims 21, 30 and 31.

For the convenience of the Examiner, Applicant has provided Figure 8F of Joshi:

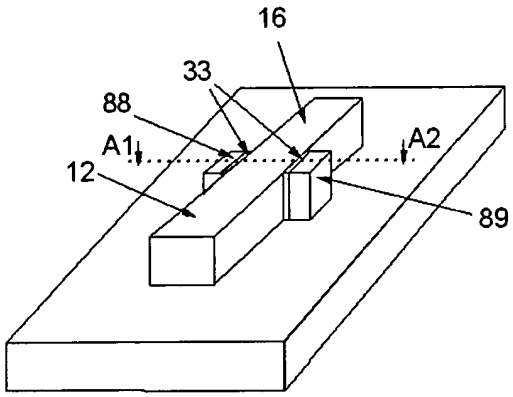
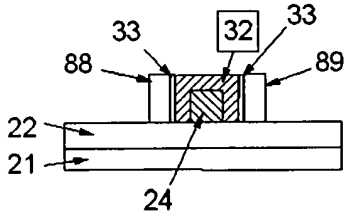


FIG. 8F (Joshi)

Furthermore, Applicant has provided a cross-sectional view through the center of the structure as indicated by the plane A1-A2 in Figure 8F, above:



A1-A2 cross-section

From right to left, plane A1-A2 cuts through gate 89, gate oxide 33, the channel envelope 32, the channel core 24, again through the channel envelope 32, gate oxide 33, and gate 88. Cross-section A1-A2 is drawn using the teaching provided by Joshi in reference to figures 8A-8F (see Joshi at col. 9, line 41 through col. 10, line 9).

Applicant points out Joshi explicitly emphasizes that "[r]egardless, each of the

embodiments of FIGS. 8A-8F may include the channel core 24 and channel envelope 32 as previously described" (see Joshi at col. 9, line 51-53). Additionally, in col. 9, lines 41 to 43 Joshi defines the channel 16 as follows "[t]he channel 16 shown in FIGS 8A-B is formed of a channel core 24 and is overlain with the channel envelope 32 as is shown in FIG. 4". Following Joshi's teaching Applicant submits that the cross-section A1-A2 provides an accurate description of the device shown in FIG. 8F.

Fig. 1, provided below, illustrates a FIN-FET structure as was first defined by Hu et al. in U.S. Patent No. 6,413,802:

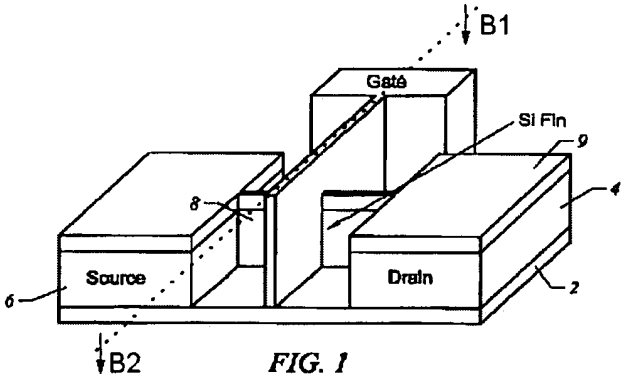
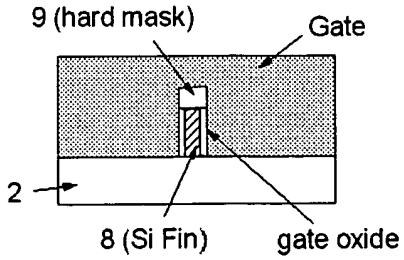


FIG. 1

FIG. 10 (Hu, US 6,413,802)

A cross-section B1-B2 through the gate shows a channel 8 made of a Si Fin:



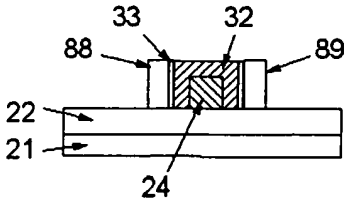
B1-B2 cross-section

Going from right to left, cross-section B1-B2 shows a gate conductor, a first gate oxide, a Si Fin, a second gate oxide, and the gate conductor. In this structure, the left side of the gate is

connected to the right side of the gate. The term "FIN-FET" as coined by Hu et al. is now broadly accepted by most electrical engineers to describe a double-gate FET formed by a thin Si fin acting as a channel and where the channel carriers are modulated from both of the channel surfaces by the gate conductor.

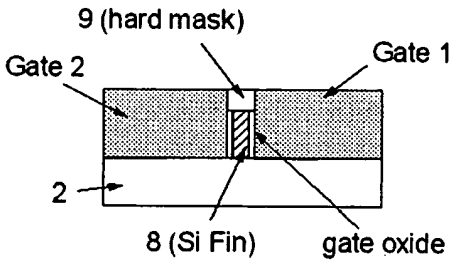
By most accepted definitions, the "FET channel" is where the sheet charge (carriers) that connects the source to the drain resides. As such, it is typically the region adjacent to the gate oxide. In typical Si FETs, this region extends form the gate oxide-Si interface to less than about 10 nm into the semiconductor (Si). As a result, double-gate FETs include a Si layer (the channel) that is about 10 nm thick and is sandwiched between a first gate and a second gate. The thin silicon layer allows each gate to control effectively the charge in the channel. A thicker silicon film will result in two parallel channels, each controlled by the gate adjacent to the gate oxide-Si interface, with little electrostatic control from the other (distant) gate. For this reason, the Fin-FET (which is a double-gate FET) includes a Si fin (the channel) that is 10 nm thick or less.

The structure of Joshi:



cross-section A1-A2
through Fig. 8F (Joshi)

is clearly different from the structure of a Fin-FET in accordance with the claimed invention:



FIN-FET

In the claimed invention, as detailed, exemplarily and schematically, above, the gate conductor was "polished" down so that two separated gates (1, 2) are formed. This "polish" of the gate conductor was taught by Joshi as the method to obtain the device of Fig. 8F from the device shown by Fig. 8C (col. 10 lines 5-9).

Channel 32 of Joshi forms an inverted U shape that warps over a core 24. The vertical portions of the outer surface of channel 32 are covered with a gate oxide 33 and are gated by gate 88 and gate 89, respectively. The inner surface of channel 32 is not gated since it is in contact with a core 24. Core 24 is not a gate, nor is there a gate oxide present between core 24 and the inner surface of channel 32.

The channel 8 (Si Fin) has two vertical surfaces. Each of these surfaces is covered with a gate oxide and is gated by gate 1 and gate 2, respectively. The carriers in the channel are therefore controlled effectively by gate 1 and gate 2. This is not the case for the carriers in channel 32 of Joshi, where the two gates are distanced by the core 24. Even if core 24 were made ultra thin, there is no gate oxide that coats the inner surface of channel 32. As a result, only one surface of the channel 32 is gated as the other (inner) surface is in contact with the core 24 and is not gated.

The above discussion explains why Joshi's structure is not a Fin-FET nor a double-gate

transistor in spite of his use of the term "Fin-FET" to describe the structure.

In view of the above discussion, the Examiner's assertion that Joshi forms a double gate based on (col. 10 line 4) is incorrect. Similarly, the assertion that "Joshi forms two gates, 88, and 89, and both sides of the channel are gated" is also incorrect, especially in view of cross-section A1-A2.

In his response (see Office Action at page 8, first paragraph) the Examiner suggests that "The applicant appears to be considering figure 4. The Examiner cites column 10 line 4 and figure 8F for Joshi's double-gate FET". Applicant again emphasizes that the numeral 16 also referred to as the "channel 16" has the same cross-section shown by Fig. 4, as taught by Joshi in col. 9 line 41 to col. 10 line 9 (see earlier discussion with respect to how cross-section A1-A2 was constructed). Thus, in Fig. 8A-8F the "channel 16" consists of a channel core 24 and is overlain with the channel envelope 32. The only difference between Fig.4 and Fig. 8 is that the structure was polished to separate the gates (col. 10, lines 5 to 8).

The Examiner argues that "the core of Joshi is part of the channel and would be then present in the final structure" (see Office Action at page 9, first paragraph). Indeed, Joshi also refers to the lumped structure of the channel envelope 32 and the channel core 24 as "channel 16" (col. 9 lines 41-43). As explained earlier, by the most accepted definitions, the "FET channel" is where the sheet charge (carriers) that connects the source to the drain resides. In view of this definition, the channel resides only in the channel envelope 32 and not in the core 24. As explained in the specification, even for a single-gate FET the presence of the stressor (the core 24 in Joshi's structure) in the final structure is not desirable. The claimed invention (e.g., as defined by claim 31) uses a stressor to induce strain in the channel. The claimed invention fixes the channel to the substrate, and later removes the stressor. The structure taught by Joshi has a channel 32 attached to a stressor 24 that remains present in the final

structure.

In the Office Action, the Examiner asks Applicant to provide proof for Applicant's assertion that when SiGe relaxes, it does so by forming defects (see Office Action at page 9, second paragraph).

This topic has been investigated for over a decade and there are many scientific papers that address SiGe relaxation. In general, "SiGe alloy layers relax by the introduction of 60° dislocations having misfit segments, which relieve the strain, lying parallel to the heterointerface, and threading segments running through the epitaxial layers." (P. M. Mooney et. al, Applied Physics Letter, 62, p. 3464, 1993). The dislocation are defects that brakes the perfect crystal structure and allow it to relax.

More recently Applicant showed that it is also possible to relax SiGe elastically (i.e. without forming defects), by making the SiGe free standing, i.e, by allowing the SiGe film to be partially detached from the substrate. The current application seeks in part to patent that method. Elastic relaxation was not discussed by Joshi, and thus it is fair to assume that when Joshi refers to a relaxed SiGe, the relaxation was achieved by plastic relaxation, i.e. by forming defects.

When Joshi cites "high quality SiGe free from dislocations" (col. 7 lines 18-19) they reference the process by which their structure was achieved: "The above process is generally known as a "smart-cut" technique, and is more particularly described by Lijuan Huang et al., Electron and Hole ... , IEEE Trans. Electron Dev., vol. 49, no 9, Sept. 2002" (see Joshi at col. 7, lines 22-27). Applicant has attached a copy of Lijuan Huang's paper.

Referring to the second paragraph in Huang's paper (SGOI MATERIAL AND DEVICE FABRICATION) the fabrication of the SiGe film is described: "*The process used to fabricate strained Si on SGOI substrates by wafer bonding is illustrated in Fig. 1.* ***Strain-relaxed SiGe***

layers with uniform Ge content in the range of 15–25% are grown by UHVCVD on (100) silicon wafers using a step-graded buffer layer approach [11]–[13]." References [11]-[13] discuss the fabrication and properties of SiGe made by the step-graded buffer layer approach. For example, in reference [12] Fitzgerald et. al report on relaxed SiGe with a dislocation density of threading dislocation densities of 10^5–5×10^6 cm^{-2}. In reference [13] K. Ismail in the introduction writes: "*The quality of epitaxially grown Si/SiGe heterostructures has improved dramatically during the past few years. In particular, the growth of strained Si imbedded between relaxed SiGe layers with a low density of misfit dislocations has become possible as a result of using a graded Ge content buffer layer*".

None of references [11]-[13] offers a dislocation free SiGe, but rather "a low density of dislocations", in the range of 10^5–5×10^6 cm^{-2}. Joshi is therefore using SiGe of high quality that is not free from dislocation, as clearly stated in Huang and related references.

Therefore, Applicants submit that there are elements of the claimed invention that are not taught or suggest by Joshi. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. NEW CLAIMS

New claims 36-38 have been added to claim additional features of the invention and to provide more varied protection for the claimed invention. These claims are independently patentable because of the novel and non-obvious features recited therein.

Applicant submits that new claims 36-38 are patentable at least based on analogous reasons to those set forth above with respect to claims 1-12, 21-24 and 28-35.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicants submit that claims 1-12, 21-24 and 28-38, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: October 11, 2006

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Electron and Hole Mobility Enhancement in Strained SOI by Wafer Bonding

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***Abstract*—N-and p-MOSFETs have been fabricated in strained Si-on-SiGe-on-insulator (SSOI) with high (15–25%) Ge content. Wafer bonding and H-induced layer transfer techniques enabled the fabrication of the high Ge content SiGe-on-insulator (SGOI) substrates. Mobility enhancement of 50% for electrons (with 15% Ge) and 15–20% for holes (with 20–25% Ge) has been demonstrated in SSOI MOSFETs. These mobility enhancements are commensurate with those reported for FETs fabricated on strained silicon on bulk SiGe substrates.**

***Index Terms*—CMOS, mobility, SiGe, silicon-on-insulator (SOI), strained silicon, wafer bending.**

I. Introduction

ELECTRON and hole mobility enhancement has been demonstrated in strained-Si MOSFETs [1]–[4]. Introducing strained Si to the silicon-on-insulator (SOI) technology promises even higher performance CMOS circuits due to the combination of carrier mobility enhancement in strained Si with the advantages of SOI devices/circuits. Strained silicon-on-SiGe-on-insulator (SGOI) has already been demonstrated by separation-by-implanted-oxygen (SIMOX) technology [5], [6]. However, previous work [5], [6] showed that it is difficult to achieve high Ge mole fraction in SGOI fabricated by SIMOX due to the high annealing temperature required for the buried oxide formation. While strain-induced electron mobility enhancement is expected to saturate at around 10% Ge, strain-induced hole mobility is expected to continue to improve significantly up to about 30% Ge [5], [7]. Thus, it is important to develop a technology to incorporate high Ge content in the relaxed SiGe on insulator. In this paper, we demonstrate an approach to prepare strained Si on SGOI with Ge contents up to 25% by wafer bonding and H-induced layer transfer techniques [8]. While earlier work [9] used a grind-and-etch-back technique and demonstrated n-MOSFETs, this paper demonstrates layer transfer of relaxed SiGe by hydrogen-induced layer splitting [8], [10]. The hydrogen-induced layer splitting improves the uniformity of the transferred SGOI layer. In addition, both N- and p-MOSFETs have been fabricated on the strained Si on SGOI in this work. Significant mobility enhancement for both electrons and holes has been demonstrated.

Manuscript received January 21, 2002; revised May 17, 2002. This paper was presented in part at the 2001 Symposium on VLSI Technology, Kyoto, Japan. The review of this paper was arranged by Editor M. Hirose.

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Publisher Item Identifier 10.1109/TED.2002.802675.

II. SGOI Material and Device Fabrication

The process used to fabricate strained Si on SGOI substrates by wafer bonding is illustrated in Fig. 1. Strain-relaxed SiGe layers with uniform Ge content in the range of 15–25% are grown by UHVCVD on (100) silicon wafers using a step-graded buffer layer approach [11]–[13]. The relaxed SiGe epilayers are implanted with hydrogen and polished by a chemical-mechanical polishing (CMP) process, which reduces the cross hatch surface roughness of the step-graded SiGe layer from 6–8 nm rms to about 0.5 nm rms as required for wafer bonding. The polished SiGe wafer is then bonded to a Si handle wafer with 300-nm thermal oxide. The bonding process includes a room temperature (RT) bonding step and an annealing step to enhance the bonding strength across the bonding interface. The RT bonding of a SiGe wafer and a Si handle wafer with SiO_2 layer is performed in class 100 clean room after standard RCA cleaning. A subsequent furnace anneal in N_2 ambient is carried out to form covalent bonds at the $SiGe/SiO_2$ interface. The annealing temperature and time are optimized to achieve a high bonding energy (>1000 mJ/m^2) while preventing separation due to H-induced surface blistering at elevated temperatures. In this work, the RT bonded wafer pairs are annealed at 250–350 °C for 20–30 h. Fig. 2 shows the transmission infra-red (IR) image of the bonded wafer pair. After the bonding anneal, another thermal anneal at higher temperatures (400–500 °C) is employed to induce the splitting process which separates the bonded wafer pair along the H peak region [8], [14]. As a result, approximately 500-nm relaxed SiGe layer is transferred onto the Si handle wafer thereby forming the SGOI substrate. The transferred 500-nm SiGe layer of the SGOI substrate is subsequently smoothed and thinned down to 200–300 nm by CMP. The surface roughness of the SGOI wafer is reduced from the as-split [Fig. 3(a)] roughness of 7.6 nm rms to the final roughness of 0.4-nm rms after CMP [Fig. 3(b)]. The final SGOI thickness may also be tailored by CMP removal of a portion of the transferred SiGe layer. A thin layer of relaxed SiGe with the same Ge mole fraction is grown on the transferred SiGe layer before the final strained silicon layer (18 nm) is grown.

Long channel, nonself-aligned n-, and p-MOSFETs with aluminum gates are fabricated on the strained Si on SGOI substrates. The channel length of the MOSFETs is in the range of 25–250 μm. The SiO_2 gate oxide is 4 nm. Phosphorous and boron are used for the source/drain doping for n- and p-FETs, respectively. Similar devices on bulk Si control substrates are also fabricated.

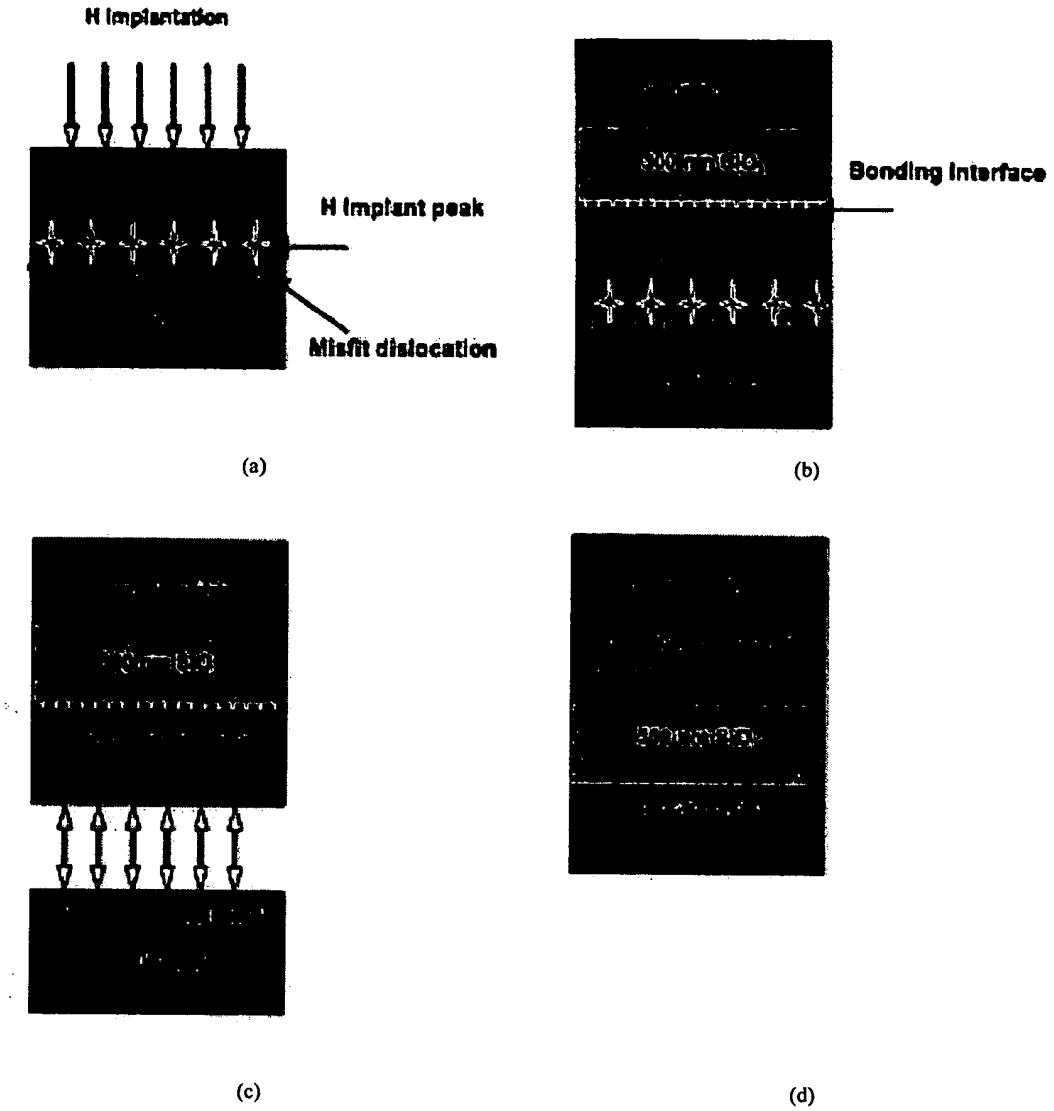

Fig. 1. Process flow for the fabrication of strained silicon on SiGe on insulator substrates.

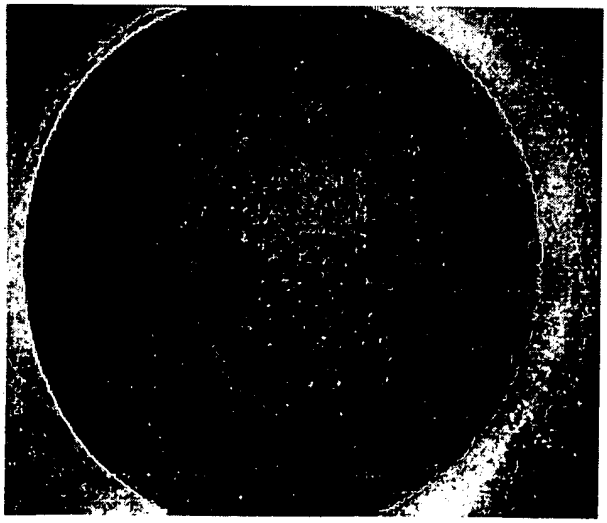

Fig. 2. Transmission infrared (IR) image of the bonded wafer pair.

Fig. 4 shows the cross-sectional SEM and TEM images of (a) the transferred and polished SiGe buffer layer, (b) the complete stack of strained silicon on the SGOI, and (c) the gate area of the completed MOSFET, showing the 4-nm gate oxide, the 18-nm strained silicon (with a light contrast), and the regrown SiGe buffer layer (with a darker contrast) on top of the transferred relaxed SiGe buffer layer. The transferred SiGe layer contains no threading dislocations in the investigated areas. The degree of relaxation in the SiGe is determined by triple-axis x-ray diffraction to be greater than 90% [Fig. 5(a)], similar to that observed in the SiGe buffer layer before the H-implant and layer splitting. This observation suggests that strain relaxation is not degraded by the layer splitting process. The strained silicon layer on the SGOI (SSOI) is more than 90% strained as deduced from Raman spectroscopy [Fig. 5(b)]. The Ge content of up to 25% in the transferred SiGe is confirmed by SIMS analysis as well as the triple-axis X-ray diffraction analysis.

III. Device Results

Typical drain current versus drain voltage output characteristics of a n- and p-FET on SSOI are given in Fig. 6. Since the capacitance–voltage (C–V) characteristics are similar to the

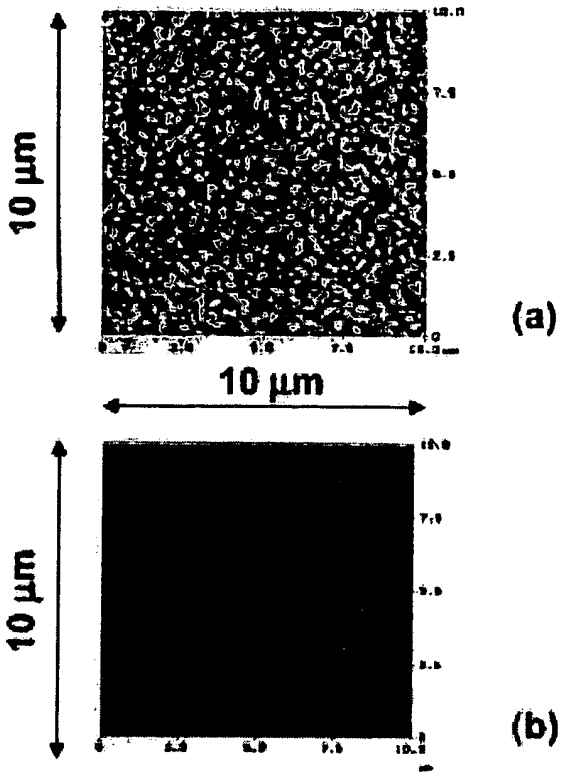

Fig. 3. AFM measurement of the surface morphology of a SiGe on insulator substrate after wafer bonding and layer-splitting by H-implant. (a) As-split, 7.6-nm rms and (b) after CMP, 0.4-nm rms.

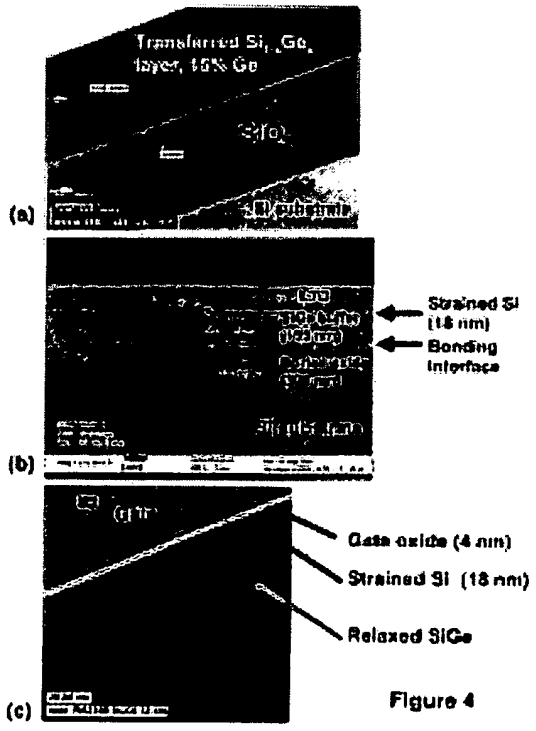

Fig. 4. (a) Cross-sectional TEM of the transferred relaxed SiGe buffer layer on the insulator substrate. (b) Cross-sectional SEM of strained silicon grown on transferred relaxed SiGe buffer layer. (c) Cross-sectional TEM of the gate area of the completed MOSFET, showing the 4-nm gate oxide, the 18-nm strained silicon (with a light contrast), and the regrown SiGe buffer layer on top of the transferred relaxed SiGe buffer layer.

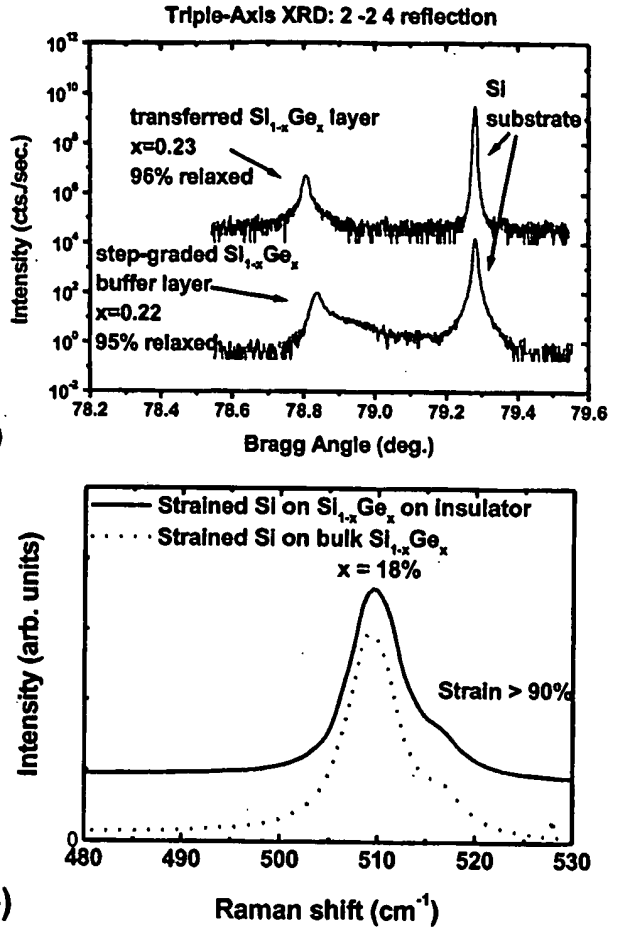

Fig. 5. (a) Triple-axis X-ray diffraction of the step-graded relaxed SiGe buffer layer and the transferred SiGe layer, each showing over 95% relaxation. (b) Raman spectroscopy of the strained silicon layer on relaxed SiGe (18% Ge) on insulator. Greater than 90% strain is obtained.

control silicon devices [see inset of Fig. 6(a)], the drain current enhancement in SSOI nFET [Fig. 6(a)] comes primarily from the increased electron mobility. The effective electron and hole mobilities are extracted based on drain current measurements at low drain voltages, with the inversion charge extracted from the C–V curve of the same device [15]. Fig. 7(a) compares the effective electron mobility in n-channel SSOI MOSFETs with that in Si control devices and the universal mobility [16]. The effective electron mobility of the SSOI device (15% Ge) is about 50% higher than that of the corresponding control-Si device as well as the universal mobility at an effective field of 1.0 MV/cm. Since earlier work on SSOI [9] and strained silicon on bulk SiGe substrates [4] showed even higher mobility enhancements, we believe further electron mobility enhancement can be obtained by process optimization such as using a conventional self-aligned polysilicon gate process to improve the gate oxide interface properties.

For p-channel SSOI MOSFETs on SGOI substrates with 20–25% Ge, the hole mobility in strained Si is 15–20% higher than the universal mobility at effective fields in the range of 0.2–0.5 MV/cm [Fig. 7(b)]. The hole mobility enhancement at higher (0.6 MV/cm) effective fields is reduced, in agreement with strained silicon FETs in bulk SiGe devices. While theory predicts continued hole mobility enhancement in strained Si

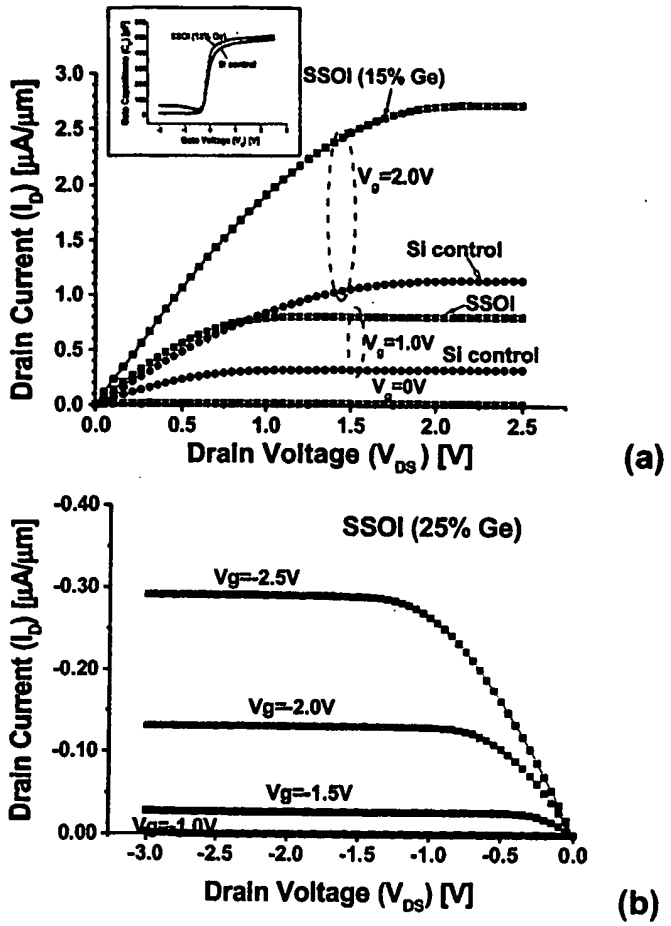

Fig. 6. Drain current versus drain voltage output characteristics of strained silicon on insulator (SSOI) MOSFETs. Channel lengths and widths are 250 μm. Gate oxide is 4 nm. (a) nFET, strained silicon on 15% relaxed SiGe. (b) pFET, strained silicon on 25% relaxed SiGe.

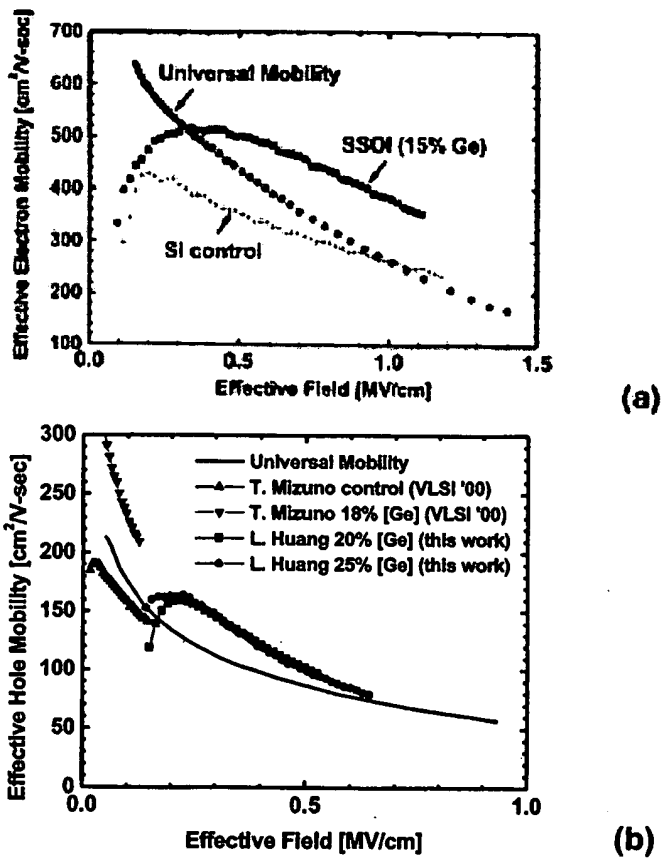

Fig. 7. Effective mobility of (a) electrons and (b) holes, measured on MOSFETs fabricated on strained silicon on SGOI substrates. The effective hole mobility data extend the effective field range reported by Mizuno *et al.* [5].

on SiGe with Ge content up to 30%, in this work, we observe only a minor difference between the hole mobility in FETs fabricated on 20% SGOI and 25% SGOI substrates. This is most probably caused by variations of the Ge fraction in our experiment. Compared to early work [5], which shows a significant hole mobility enhancement over universal hole mobility but achieved at lower effective fields (<0.1 MV/cm), this work demonstrates hole mobility enhancement in strained Si at higher vertical fields (up to 0.6 MV/cm).

IV. Conclusions

Relaxed SiGe-on-insulator (SGOI) substrates with 15–25% Ge content have been fabricated by wafer bonding and hydrogen-induced layer transfer techniques. N- and p- MOSFETs have been fabricated in strained Si on SiGe on insulator (SSOI) substrates with high Ge content. Mobility enhancement of 50% for electrons (with 15% Ge) and 15–20% for holes (with 20–25% Ge) have been demonstrated. The effective electron and hole mobility enhancements for FETs fabricated on strained silicon on SiGe on insulator substrates are comparable to the mobility enhancements obtained in strained silicon FETs on bulk SiGe substrates. The wafer bonding and hydrogen-induced layer transfer process employed to fabricate SiGe on insulator have not degraded the quality of the starting relaxed SiGe layer. This work suggests that it is possible to combine the benefits of electron and hole mobility enhancements in strained Si and the advantages of SOI technology for high-speed CMOS.

Acknowledgment

The authors would like to thank J. Cai, G. Cohen, M. Ieong, T. Ning, C. Ouyang, K. Rim, and Y. Taur for their stimulating discussions and support. Devices were fabricated with support from ASTL/S and CSS. The management support of J. Dukovic, A. Grill, M. Krishnan, D. Seeger, and J. Warlaumont is greatly appreciated.

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